Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for controlling access to a dynamic random access memory (DRAM) arranged in a computer system having a processor controlled by a microcode instruction program, and a memory controller, wherein said method comprises the step of performing, for each DRAM access, a sequence of a predetermined number of DRAM control operations, ~~each DRAM control operation being~~ in response to a corresponding sequence of control instructions included in microcode instructions of said microcode program of the processor, wherein each DRAM control operation corresponds to a predetermined sub cycle of a DRAM access so that an entire sequence of DRAM control operations is required for a complete DRAM access.

2. (Previously presented) The method according to claim 1, wherein each microcode instruction includes a control instruction, formed by at least one control bit, controlling which one of a plurality of predefined DRAM control operations to perform.

3. (Previously presented) The method according to claim 2, wherein said predefined DRAM control operations are arrangeable to form said sequence of DRAM control operations such that a read access, a write access, a page mode read access, a page mode write access, a page mode read write access or a page mode write read access to said DRAM is enabled.

4. (Previously presented) The method according to claim 1, wherein at least one control instruction in said sequence of control instructions temporarily puts the memory cycle of said DRAM on hold.

5. (Previously presented) The method according to claim 1, wherein said method further comprises the step of selecting the cycle time of each microcode instruction from a number of different cycle times such that the cycle time of each microcode instruction matches the duration of the corresponding DRAM control operation.

6. (Previously presented) The method according to claim 5, wherein each microcode instruction includes a cycle time control bit determining the cycle time of the microcode instruction, a first logical state of the cycle time control bit indicating a first cycle time and a second logical state of the cycle time control bit indicating a second extended cycle time.

7. (Previously presented) The method according to claim 2, wherein a first one, referred to as an R-operation, of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

selectively enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and, a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal.

8. (Previously presented) The method according to claim 2,
wherein a second one, referred to as a W-operation, of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said

DRAM;

selectively, if inactive, activating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and, a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal.

9. (Previously presented) The method according to claim 2, wherein a third one, referred to as a H-operation, of said predefined DRAM control operations includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and

deactivating a write enable signal to said DRAM.

10. (Previously presented) The method according to claim 2, wherein a fourth one, referred to as an E-operation, of said predefined DRAM control operations includes the steps of:

deactivating a row address strobe (RAS) signal to said DRAM;

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

enabling a valid row address to be forwarded to said DRAM.

11. (Previously Presented) The method according to claim 2, wherein an R-operation of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

selectively enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and, a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal;

wherein an H-operation of said predefined DRAM control operations includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and

deactivating a write enable signal to said DRAM;

wherein an E-operation of said predefined DRAM control operations includes the steps of:

deactivating a row address strobe (RAS) signal to said DRAM;

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM; and

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

enabling a valid row address to be forwarded to said DRAM; and

wherein, for a read access to said DRAM, said sequence of DRAM control operations includes an R-operation, an H-operation and an E-operation, in that order.

12. (Previously Presented) The method according to claim 2, wherein a W-operation of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said DRAM;

selectively, if inactive, activating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and, a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal;

wherein an H-operation of said predefined DRAM control operations includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and

deactivating a write enable signal to said DRAM;

wherein an E-operation of said predefined DRAM control operations includes the steps of:

deactivating a row address strobe (RAS) signal to said DRAM;

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

enabling a valid row address to be forwarded to said DRAM; and

wherein, for a write access to said DRAM, said sequence of DRAM control operations includes a W-operation, an H-operation and an E-operation, in that order.

13. (Previously presented) The method according to claim 2, wherein an R-operation of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

selectively enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal;

wherein an H-operation of said predefined DRAM control operations includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and

deactivating a write enable signal to said DRAM;

wherein yet another one, referred to as an E-operation, of said predefined DRAM control operations includes the steps of:

deactivating a row address strobe (RAS) signal to said DRAM;

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

enabling a valid row address to be forwarded to said DRAM; and

wherein, for a page mode read access to said DRAM, said sequence of DRAM control operations includes a predetermined number of R-operations followed by an H-operation and an E-operation.

14. (Previously Presented) The method according to claim 2, wherein a W-operation of said predefined DRAM control operations includes the steps of:

selectively, if inactive, activating a row address strobe (RAS) signal to said DRAM;

enabling a valid row address to be forwarded to said DRAM, and, a first predetermined period of time later, enabling a valid column address to be forwarded to said DRAM;

selectively, if inactive, activating a write enable (WE) signal to said DRAM; and

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM, and, a second predetermined period of time later, in the next microinstruction cycle, activating said CAS signal;

wherein an H-operation of said predefined DRAM control operations includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and

deactivating a write enable signal to said DRAM;

wherein an E-operation of said predefined DRAM control operations includes the steps of:

deactivating a row address strobe (RAS) signal to said DRAM;

selectively, if active, deactivating a column address strobe (CAS) signal to said DRAM;

selectively, if active, deactivating a write enable (WE) signal to said DRAM; and

enabling a valid row address to be forwarded to said DRAM; and wherein, for a page mode write access to said DRAM, said sequence of DRAM control operations includes a predetermined number of W-operations followed by an H-operation and an E-operation.

15. (Currently amended) A controller for a dynamic random access memory (DRAM) in a computer system having a processor with a processor control unit implemented by a microcode program, wherein said DRAM controller is ~~responsive to a sequence of control instructions for controlling access to said DRAM, each control instruction being included in a microcode instruction of a processor~~ operable for executing, for each DRAM access, a sequence of DRAM control operations in response to a corresponding sequence of control instructions included in microcode instructions of said microcode program, each DRAM control operation corresponds to a predetermined sub cycle of a DRAM access so that an entire sequence of DRAM control operations is required for a complete DRAM access.

16. Cancelled.

17. (Previously presented) The DRAM controller according to claim 15, wherein each control instruction, formed by at least one control bit, controls which one of a plurality of predefined DRAM control operations to perform.

18. (Currently amended) The DRAM controller according to claim 15 ~~16 or 17~~, wherein the cycle time of each microcode instruction is extendable such that the cycle time of each microcode instruction matches the duration of the corresponding DRAM control operation.

19. (Previously presented) The DRAM controller according to claim 18, wherein the cycle time of each microcode instruction is extendable by means of a cycle time control instruction included within the microcode instruction itself.

20. (Previously presented) The DRAM controller according to claim 15, wherein at least one control instruction in said sequence of control instructions temporarily puts the memory cycle of said DRAM on hold.

21. (Previously presented) The DRAM controller according to claim 15, wherein the microcode instructions of said processor are stored in a program memory separated from said DRAM.

22. (Previously presented) The DRAM controller according to claim 15, wherein said DRAM controller is responsive to address information, determined by a number of microcode instructions of said processor, for addressing said DRAM.

23. (Previously presented) The DRAM controller according to claim 15, wherein the microcode instructions of said processor are the instructions of a reduced instruction set computing (RISC) processor.

24. (Currently amended) A computer system having a processor controlled by a microcode instruction program, a primary memory cooperating with said processor, and a memory

controller for said primary memory,

wherein said microcode program comprises microcode instructions, each microcode instruction having a special control instruction field holding a control instruction for memory access control; and

wherein said memory controller is ~~responsive to a sequence of control instructions from said processor for controlling access to said primary memory, each control instruction being included in a microcode instruction of said processor~~operable for executing, for each memory access, a sequence of memory control operations in response to a corresponding sequence of control instructions from said processor, each memory control operation corresponds to a predetermined sub cycle of a memory access, and an entire sequence of memory control operations is required for a complete memory access.

25. (Previously presented) The computer system according to claim 24, wherein said primary memory is a DRAM, and said memory controller controls access to said DRAM by performing a sequence of DRAM control operations in response to said sequence of control instructions.

26. (Previously presented) The computer system according to claim 25, wherein said processor and said DRAM are provided on the same circuit board.

27. (Previously presented) The computer system according to claim 24, wherein said processor is a complex instruction set computing (CISC) processor, and complex instructions are stored in said primary memory and executed by microcode instructions stored in a program memory in said processor.

28. (Previously presented) The computer system according to claim 25, wherein the cycle time of each microcode instruction is extendable such that the cycle time of each microcode instruction matches the duration of the corresponding DRAM control

operation.

29. (Currently amended) A method for performing a virtual direct memory access (DMA) to a primary memory in a computer system having a processor controlled by a microcode instruction program, wherein said method comprises the steps of:

storing data from/to ~~an~~ a peripheral input/output device in a buffer;

transferring said data between said buffer and said primary memory via internal data paths of the ~~a~~ processor of the computer system, said data transfer being controlled by said ~~a~~ microcode instruction program of the processor,

wherein said step of transferring data between said buffer and said primary memory includes the step of executing, for each access to said primary memory, a sequence of memory control operations in response to a corresponding sequence of control instructions included in microcode instructions of said microcode instruction program, each memory control operation corresponds to a predetermined sub cycle of a memory access, and an entire sequence of memory control operations is required for a complete memory access.

30. (Currently amended) The method for performing a virtual DMA access to a primary memory according to claim 29,

wherein said step of transferring data between said buffer and said primary memory includes the steps of:

transferring data between said buffer and an internal register of said processor in response to control signals generated by said microcode instruction program; and

transferring data between said internal register and said primary memory in response to ~~a~~said sequence of control instructions included in microcode instructions of said microcode instruction program.

31. (Currently amended) The method for performing a virtual DMA access to a primary memory according to claim 30, wherein said primary memory is a dynamic random access

memory (DRAM), and said step of transferring data between said internal register and said DRAM includes performing a sequence of DRAM control operations in response to, ~~each DRAM control operation being included in~~ said sequence of control instructions.

32. (Previously presented) The method for performing a virtual DMA access to a primary memory according to claim 29,

wherein said method further comprises the step of regularly investigating whether a predetermined amount of data is present in said buffer for inputs to the primary memory, and whether there is a predetermined amount of free space available in said buffer for outputs from the primary memory, said transfer between said buffer and said primary memory being initiated in dependence upon the outcome of said investigation.

33. (Previously presented) The method for performing a virtual DMA access to a primary memory according to claim 32,

wherein said investigating step is performed by at least one microcode instruction that is activated at a predetermined frequency.

34. (Previously presented) The method for performing a virtual DMA access to a primary memory according to claim 29,

wherein said method further comprises at least one of processing and monitoring, in said processor, of data transferred between said buffer and said primary memory via said internal data paths of said processor.

35. (Previously presented) The method for performing a virtual DMA access to a primary memory according to claim 34,

wherein said processing comprises at least one of the following: data conversion, data encoding, data decoding, image data compression, image data decompression, scaling, pattern matching and checksum calculation.

36. (Currently amended) A computer system having a processor controlled by a microcode instruction program and a primary memory coupled to said processor, wherein said computer system further comprises:

a buffer for storing data from/to ~~an~~ a peripheral input/output device; and

means for transferring said data between said buffer and said primary memory via internal data paths of the processor under the control of saida microcode instruction program in the processor,

wherein said means for transferring data between said buffer and said primary memory includes means for executing, for each access to said primary memory, a sequence of memory control operations in response to a corresponding sequence of control instructions included in microcode instructions of said microcode instruction program, each memory control operation corresponds to a predetermined sub cycle of a memory access, and an entire sequence of memory control operations is required for a complete memory access.

37. (Previously presented) The computer system according to claim 36, wherein said means for transferring data between said buffer and said primary memory includes:

means for transferring data between said buffer and an internal register of said processor in response to control signals generated by said microcode instruction program; and

means for transferring data between said internal register and said primary memory in response to a sequence of control instructions included in microcode instructions of said microcode instruction program.

38. (Previously presented) The computer system according to claim 37, wherein said means for transferring data between said buffer and said internal register includes a DMA controller, which also controls transfer of data between said input/output device and said buffer.

39. (Previously presented) The computer system according to claim 37, wherein said primary memory is a dynamic random access memory (DRAM), and said means for transferring data between said internal register and said DRAM includes a DRAM controller for performing a sequence of DRAM control operations in response to said sequence of control instructions.

40. (Previously presented) The computer system according to claim 36, wherein said microcode instruction program of said processor is configured for performing at least one of processing and monitoring of data transferred between said buffer and said primary memory via the internal data paths of said processor.

41. (Previously presented) The computer system according to claim 40, wherein said processing comprises at least one of the following: data conversion, data encoding, data decoding, image data compression, image data decompression, scaling, pattern matching and checksum calculation.

42. - 45. (Not entered)